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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,558	01/22/2002	Jiin Lai	JCLA7148	6096

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EXAMINER	
CERULLO, JEREMY S	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,558	LAI ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this action.

Specification

2. The disclosure is objected to because of the following informalities: In the title of the invention, to be consistent with the rest of the disclosure, the word "briding" should apparently be "bridging".

Appropriate correction, if necessary, is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,081,851 ("Futral" et al.). AAPA teaches a method of sequencing data transmission inside a computer system, wherein the computer system has a bridging device (Figure 1, Item 180), a first bus (Figure 1, Item 100) and a second bus (Figure 1, Item 110), and the bridging device includes a second-to first write buffer (Figure 1, Item 130). The method comprises the recording a plurality of write data stored inside the write buffer (Figure 2, SP_w[1:0]) when first-to-second read operation (Figure 2, PS_r_a) occurs, and transmitting the response data to the first bus after transmitting the write data to the first bus (Figure 2, PS_r_d). AAPA does not explicitly teach that the bridging device holds the response data after executing the read operation on the second bus, but it known in the art that the bridging device must have some way to hold/transmit the data from one bus to another. Futral teaches that this may be accomplished through the use of a read buffer (Column 1, Line 60 – Column 2, Line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a read buffer as taught by Futral to hold the data in the bridging device of AAPA to prevent both of the buses from having to wait (idle) until the read data was read to be transmitted.

6. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Futral as applied to claim 1 above, and further in view of U.S. Patent No. 5,588,125 ("Bennett").

7. As for Claim 5, AAPA and Futral teach all of the limitations inherited from Claim 1, but they do not teach the use of a counter within the bridging device. However, Bennett does teach the use of a counter that keeps track of the amount of data stored in a posted write buffer (Figure 2, Item 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a counter as taught by Bennett in the method taught by AAPA and Futral in order to determine if all of the data was out of the buffer before performing the read operation.

8. As for Claim 6, Bennett teaches the additional limitation that the counter (Figure 2, Item 56) sends out a control signal (Figure 2, Item 76) when all of the write data has been written, i.e. the write buffers are empty.

9. As for Claims 2-3, in paragraph [0020] of the instant application, the applicant admits that the flush flag buffer and the block logic can be implemented as a counter for storing the amount of data in the write buffers that allows the data in the hold buffer to be transmitted when the counter reaches zero. Therefore, Claims 2-3 are rejected on the same basis as Claims 5-6.

10. As for Claim 4, Futral teaches the use of a read buffer in the bridging device for holding the response data (See Rejection of Claim 1 above).

11. As for Claim 7, Futral teaches the use of a read buffer in the bridging device for holding the response data (See Rejection of Claim 1 above).

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,081,851 ("Futral" et al.). AAPA teaches a bridging device (Figure 1, Item 180) coupled to a first bus (Figure 1, Item 100) and a second bus (Figure 1, Item 110), and the bridging device includes a second-to first write buffer (Figure 1, Item 130). The bridging device records a plurality of write data stored inside the write buffer (Figure 2, SP_w[1:0]) when first-to-second read operation (Figure 2, PS_r_a) occurs, and transmits the response data to the first bus after it transmits the write data to the first bus (Figure 2, PS_r_d). AAPA does not explicitly teach that the bridging device holds the response data after executing the read operation on the second bus, but it known in the art that the bridging device must have some way to hold/transmit the data from one bus to another. Futral teaches that this may be accomplished through the use of a read buffer (Column 1, Line 60 – Column 2, Line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a read buffer as taught by Futral to hold the data in the bridging device of AAPA to prevent both of the buses from having to wait (idle) until the read data was read to be transmitted.

13. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Futral as applied to claim 8 above, and further in view of U.S. Patent No. 5,588,125 ("Bennett").

14. As for Claim 12, AAPA and Futral teach all of the limitations inherited from Claim 8, but they do not teach the use of a counter within the bridging device. However,

Bennett does teach the use of a counter that keeps track of the amount of data stored in a posted write buffer (Figure 2, Item 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a counter as taught by Bennett in the method taught by AAPA and Futral in order to determine if all of the data was out of the buffer before performing the read operation.

15. As for Claim 13, Bennett teaches the additional limitation that the counter (Figure 2, Item 56) sends out a control signal (Figure 2, Item 76) when all of the write data has been written, i.e. the write buffers are empty.

16. As for Claims 9-10, in paragraph [0020] of the instant application, the applicant admits that the flush flag buffer and the block logic can be implemented as a counter for storing the amount of data in the write buffers that allows the data in the hold buffer to be transmitted when the counter reaches zero. Therefore, Claims 9-10 are rejected on the same basis as Claims 12-13.

17. As for Claim 11, AAPA teaches that the read response data cannot be transmitted until the write buffers are empty, and Bennett teaches that his counter indicates that the write buffers are empty. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the control signal output by the counter to control the output of the read buffer.

18. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,081,851 ("Futral" et al.). AAPA teaches a data transmission sequencing system, wherein the system has a

bridging device (Figure 1, Item 180), a first bus (Figure 1, Item 100) and a second bus (Figure 1, Item 110), and the bridging device includes a second-to first write buffer (Figure 1, Item 130). The bridging device records a plurality of write data stored inside the write buffer (Figure 2, SP_w[1:0]) when first-to-second read operation (Figure 2, PS_r_a) occurs, and transmits the response data to the first bus after it transmits the write data to the first bus (Figure 2, PS_r_d). AAPA does not explicitly teach that the bridging device holds the response data after executing the read operation on the second bus, but it known in the art that the bridging device must have some way to hold/transmit the data from one bus to another. Futral teaches that this may be accomplished through the use of a read buffer (Column 1, Line 60 – Column 2, Line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a read buffer as taught by Futral to hold the data in the bridging device of AAPA to prevent both of the buses from having to wait (idle) until the read data was read to be transmitted.

19. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Futral as applied to claims 14-15 above, and further in view of U.S. Patent No. 5,588,125 ("Bennett").

20. As for Claim 19, AAPA and Futral teach all of the limitations inherited from Claims 14-15, but they do not teach the use of a counter within the bridging device. However, Bennett does teach the use of a counter that keeps track of the amount of data stored in a posted write buffer (Figure 2, Item 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a counter as

taught by Bennett in the method taught by AAPA and Futral in order to determine if all of the data was out of the buffer before performing the read operation.

21. As for Claim 20, Bennett teaches the additional limitation that the counter (Figure 2, Item 56) sends out a control signal (Figure 2, Item 76) when all of the write data has been written, i.e. the write buffers are empty.

22. As for Claims 16-17, in paragraph [0020] of the instant application, the applicant admits that the flush flag buffer and the block logic can be implemented as a counter for storing the amount of data in the write buffers that allows the data in the hold buffer to be transmitted when the counter reaches zero. Therefore, Claims 16-17 are rejected on the same basis as Claims 19-20.

23. As for Claim 18, AAPA teaches that the read response data cannot be transmitted until the write buffers are empty, and Bennett teaches that his counter indicates that the write buffers are empty. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the control signal output by the counter to control the output of the read buffer.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 5,202,969; U.S. Patent No. 5,579,530; U.S. Patent No. 6,433,785; U.S. Patent No. 6,460,114.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571) 272-3634. The examiner can normally be reached on Monday - Thursday, 7:00-4:30; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JSC

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